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DOCKET NO: GSH 08-886639

DATE: July 17, 2000

COMMISSIONER OF PATENTS & TRADEMARKS
WASHINGTON, D.C. 20231

Dear Sir:

Transmitted herewith for filing is the patent application of:

INVENTORS: Paul HUA and Peter HAUDEROWICZ

FOR: ACTIVE PIXEL SENSOR ARRAY RESET

Enclosed are the following:

- Specification: 8 pages; Claims: 2 pages; Abstract: 1 page
- Declaration and Power of Attorney
- Sheet(s) of drawings 4 pages
- An assignment of the invention to: Semiconductor Insights, Inc.
- A verified statement to establish small entity status
- Prior Art Disclosure Statement

The filing fee has been calculated as shown below:

		SMALL ENTITY	LARGE ENTITY
BASIC FEE:		$345.00	$690.00
TOTAL CLAIMS:	8 - 20 =	x 9 = $	x 18 = $
INDEPENDENT CLAIMS:	2 - 3 =	x 39 = $	x 78 = $
MULT. DEPEND. CLAIMS:		+ 130 = $	+ 260 = $
TOTAL:		$345.00	$

- Please charge the Credit Card in the amount of $ 385.00 ($40.00 Assignment recordal fee included) as indicated on Form PTO-2038 enclosed.

The Commissioner is hereby authorized to charge any additional filing fees required under 37 CFR 1.16 or credit any overpayment to Deposit Account No. 08-1391.

Norman P. Soloway
Attorney for Applicant
Reg. No. 24,315

clm

CERTIFICATE OF EXPRESS MAILING

"Express Mail" Mailing Label No: EL518277950US
Date of Deposit: July 17, 2000

I hereby certify that this paper and the papers listed thereon are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above, and is addressed to BOX PATENT APPLICATION, Assistant Commissioner of Patents, Washington, DC 20231.

Signature of person mailing: Kristine Stevens
Name of person mailing:

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

☒ In re application of: **Paul HUA; and Peter HAUDEROWICZ**

Serial No.: Group No.:
Filed: Examiner:

For*: ***ACTIVE PIXEL SENSOR ARRAY RESET***

☐ Patent No.: Issued:

*NOTE: *Insert name(s) of inventor(s) and title also for patent. Where statement is with respect to a maintenance fee payment also insert application serial number and filing date and add Box M. Fee to address.*

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS (37 CFR 1.9(c-f) AND 1.27(b-d))

With respect to the invention described in

☒ the specification filed herewith.
☐ application serial no. _____, filed _____

☐ patent no. _____, issued _____

I. IDENTIFICATION OF DECLARANT AND RIGHTS AS A SMALL ENTITY

I hereby declare that I am

(complete either (a), (b), (c) or (d) below):

(a) Independent Inventor

☐ a below named independent inventor and that I qualify as an independent inventor as defined in 37 CFR 1.9(c) for purposes of paying reduced fees under Section 41(a) and (b) of Title 35, United States Code to the Patent and Trademark Office.

(b) Non-inventor Supporting a Claim by Another

☐ making this verified statement to support a claim by

_____

for a small entity status for purposes of paying reduced fees under Section 41(a) and (b) of Title 35, United States Code and I hereby declare that I would qualify as an independent inventor as defined in 37 CFR 1.9(c) for purposes of paying reduced fees under 41(a) and (b) of Title 35, United States Code, if I had made the above identified invention.

(c) Small Business Concern

☐ the owner of the small business concern identified below:
☑ an official of the small business concern empowered to act on behalf of the concern identified below:

Name of Concern Semiconductor Insights Inc.
Address of Concern 3000 Solandt Road, Kanata, Ontario, K2K 2X2, CANADA
and that the above identified small business concern qualifies as a small business concern as defined in 13 CFR 121.3-18, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees under Section 41(a) and (b) of the Title 35, United States Code, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

(d) Non-Profit Organization

☐ an official empowered to act on behalf of the non-profit organization identified below:

NAME OF ORGANIZATION _____
ADDRESS OF ORGANIZATION _____
_____

TYPE OF ORGANIZATION

☐ UNIVERSITY OR OTHER INSTITUTION OF HIGH EDUCATION
☐ TAX EXEMPT UNDER INTERNAL REVENUE SERVICE CODE (26 USC 501(a) and 501(c) (3))
☐ NON-PROFIT SCIENTIFIC OR EDUCATIONAL UNDER STATUTE OF STATE OF THE UNITED STATES OF AMERICA
(NAME OF STATE _____)
(CITATION OF STATUTE _____)
☐ WOULD QUALIFY AS TAX EXEMPT UNDER INTERNAL REVENUE SERVICE CODE (26 USC 501(a) and 501(c) (3)) IF LOCATED IN THE UNITED STATES OF AMERICA
☐ WOULD QUALIFY AS NON-PROFIT SCIENTIFIC OR EDUCATIONAL UNDER STATUTE OF STATE OF THE UNITED STATES OF AMERICA IF LOCATED IN THE UNITED STATES OF AMERICA
(NAME OF STATE _____)
(CITATION OF STATUTE _____)

and that the non-profit organization identified above qualifies as a non-profit organization as defined in 37 CFR 1.9(e) for purposes of paying reduced fees under Section 41(a) and (b) of Title 35, United States Code.

II. OWNERSHIP OF INVENTION BY DECLARANT

I hereby declare that rights under contract or law remain with and/or have been conveyed to the above identified

☐ person	☒ concern	☐ organization
(item (a) or (b) above	(item (c) above)	(item (d) above)

EXCEPT, that if the rights held are not exclusive, each individual, concern or organization having rights to the invention is listed below* and no rights to the invention are held (1) by any person who could not be classified as an independent inventor under 37 CFR 1.9(c) if that person had made the invention, (2) any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or (3) a non-profit organization under 37 CFR 1.9(e).

☐ no such person, concern, or organization
☐ person, concerns or organizations listed below*

*NOTE: *Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)*

FULL NAME _____
ADDRESS _____
_____

☐ Individual ☐ Small Business Concern ☐ Non-Profit Organization

FULL NAME _____
ADDRESS _____
_____

☐ Individual ☐ Small Business Concern ☐ Non-Profit Organization

III. ACKNOWLEDGEMENT OF DUTY TO NOTIFY PTO OF STATUS CHANGE

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

IV. DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

V. SIGNATURES

(complete only (e) or (f) below)

(e)
Note: All inventors must sign the verified statement

____
Name of Inventor

____________________________________ ________________________________
Signature of Inventor Date

or

(f)
Note: The title of the person signing on behalf of a concern or non-profit organization should be specified.

NAME OF PERSON SIGNING DOUG SMEATON
TITLE OF PERSON PRES. & C.E.O.

(if signing on behalf of a concern or non-profit organization)

ADDRESS OF PERSON SIGNING 1526 MONAGHAN LANE
KANATA, ONTARIO.

SIGNATURE [signature] DATE JULY 13/00

ACTIVE PIXEL SENSOR ARRAY RESET

Field of the Invention

The invention relates generally to image sensing circuits, and more particularly to the resetting of active pixel sensor arrays.

Background of the Invention

CMOS image sensor arrays can employ several types of pixels. Passive pixel sensor cells are comprised of a simple photodiode and an access transistor. Active pixel sensor (APS) cells have added features including a reset transistor and a source follower amplifier.

A conventional APS sensing array is composed of individual light sensitive transducers called pixels that are organized in rows and columns. One typical pixel arrangement is composed of a photodiode (with junction capacitance), a reset transistor with a reset gate, an amplifier transistor, and a row select transistor.

During the reset cycle, charge is transferred onto the capacitive element through the reset transistor. An integration cycle allows charge from the capacitive element to be discharged through the photodiode. The remaining charge is then sampled by the amplifying gate and transferred to column amplifiers through the row select transistor. Upon completion of this cycle, the capacitive element in the array must be reset via the reset transistor. At this moment, a substantial amount of charge can be driven onto the substrate, raising the substrate bias voltage. Since the substrate is common for both the sensor array and peripheral circuitry, a significant increase in substrate charge increases the substrate bias voltage, which in turn can cause a circuit malfunction referred to as latch-up.

Latch-up is defined as the generation of a low-impedance path in CMOS devices between the power supply rail and the ground rail. It is a well known fact that, under certain conditions, a parasitic PNPN junction can be created in a CMOS integrated circuit, resulting in the latch-up and possibly destruction of the CMOS integrated circuit.

Latch-up is a parasitic conduction mechanism to which CMOS structures have an inherent vulnerability. It is a thyristor operating mechanism that can be triggered in PNPN structures. If any such PNPN structure is triggered into latch-up on a chip, large currents can flow and the results are usually irreversibly catastrophic for the entire chip.

Traditionally, integrated circuit designers have often relied on the fact that, typically, the operating characteristics of a CMOS integrated circuit are insufficient to surpass the high current threshold for triggering a latch-up. The potential problem is evaded by placing many substrate connections around the circuit. The substrate connections can draw off any potential current overload and prevent the latch-up triggering. However, in imaging circuitry, the fill factor, or percentage of the total pixel real estate that is effectively photosensitive, is significantly reduced if substrate connections were to be integrated within the cell. It is therefore impractical to place substrate connections within the array. In conventional APS imaging arrays the array size and the amount of charge being discharged upon reset is insufficient to cause latch-up, but due to the increasing size of sensor arrays, (1.3Mpixels), the charge increase must be considered.

Several methods are used to prevent circuit latch-up, including well definition and the reduction of the lateral resistance of the n-tub. Well definition can effectively prevent PNPN junction formation particularly for small circuits; however, the amount of charge related to an array reset can be too great for sufficient latch-up prevention using the well definition method. Since the presence of large lateral resistance in the n-tubs has been found to cause latch-up, it was felt that the reduction of lateral resistance may prevent latch-up. Although this method is proven to be effective, it cannot handle large currents.

Additionally, a change in the process for semiconductor substrates also increases costs, which should be minimized for production.

United States Patent No. 5,881,184 which was issued on March 9, 1999, describes a pixel for an imager in which the reset transistor either has two functions or is replaced by two reset transistors. In the latter case, the only way that the pixel can be reset is if a reset signal is applied to the gates of both of the transistors. The advantage of this is that each pixel can be reset individually rather then having all of the pixels in a row reset at the same time. This reference does not address the problem of the occurrence of latch-up during pixel resetting.

Therefore, there is a need for a method and apparatus for safely resetting active pixel sensor arrays without a significant increase in current that may cause destructive latch-up.

Summary of the Invention

The invention is directed to a method and apparatus resetting an array of active pixel sensors (APS) arranged in rows and columns on a substrate.

In accordance with one aspect of this invention, the resetting process comprises the sequential pre-resetting of groups of one or more sensors in the array and then simultaneously resetting all of the sensors. The groups may be formed from one or more adjacent or non-adjacent individual sensors, rows or columns of sensors. The process may further include the step of detecting the bias voltage present on the array substrate to determine the number of sensors in the groups being pre-reset.

In accordance with another aspect of this invention, the apparatus for resetting the array of active pixel sensors which are arranged in rows and columns comprises a controller which is coupled to the sensor array for applying signals to the array for sequentially pre-resetting groups of one or more sensors in the array and then for simultaneously applying a signal to all of the sensors in the sensor array for resetting the

entire array. The apparatus may further include a detector for sensing the bias voltage of the sensor array substrate for the controller to determine the number of sensors in each group being pre-reset. The groups of sensors being pre-reset may include one or more adjacent or non-adjacent individual sensors or rows or columns of sensors.

Other aspects and advantages of the invention, as well as the structure and operation of its various embodiments, will become apparent to those ordinarily skilled in the art upon review of the following description in conjunction with the accompanying drawings.

Brief Description of the Drawings

The invention will be described with reference to the accompanying drawings, wherein:

Figure 1 is a block diagram of a typical image sensor array;

Figure 2 is a circuit diagram of an active pixel sensor (APS) cell;

Figure 3 illustrates a block diagram of the sensor array in accordance with the present invention; and

Figure 4 illustrates a block diagram of the sensor array of a further embodiment of the present invention including bias voltage sensing means.

Detailed Description of the Invention

Referring to figure 1, there is shown a block diagram of a typical image sensor array 10. The sensor array 10 consists of active pixel sensor (APS) cells 11 arranged in rows 1 to n and columns 1 to m. The columns 1 to m of APS cells 11 are provided a voltage Vdd from a voltage supply 12 through lines VR_1 to VR_m. In addition, each row 1 to n of APS cells 11 simultaneously receive reset enable signals RRE_1 to RRE_n from a reset signal 13 on lines 14_1 to 14_n to reset the sensor circuits 11. Access to each horizontal row 1 to n of APS cells 11 is provided by applying individual access signals

RA_1 to RA_n which are normally pulses of equal amplitude but spaced in time via row lines 15_1 to 15_n from a row address decoder 16. The columns 1 to m of APS cells 11 are connected via data lines DL_1 to DL_m which are coupled to column sense amplifiers 17 to amplify the image signal. Thus the rows 1 to n of cells 11 are simultaneously reset by signals RRE_1 to RRE_n for sensing the incident light on the cells 11 whereas the sequential detecting of the level of incident light in the rows 1 to n of cells 11 is initiated by access signals RA_1 to RA_n and received on data lines DL_1 to $DL_{m.}$

A typical three transistor APS cell 11 is illustrated in figure 2. The cell 11 consists of a photodiode 21 which is inherently in parallel with a diffusion 26 acting as a capacitor coupled to the source of a reset transistor 22 and the gate of a transistor 23 which acts as a source follower amplifier. The drains of the reset transistor 22 and of the amplifying transistor 23 are normally connected to a supply voltage Vdd through a voltage line $VR_{m,}$ however the reset transistor 22 and the amplifying transistor 23 may be connected to different voltage sources. The amplifying transistor 23 source is coupled to a data line DL_m through an access transistor 24. When activated, the reset transistor 22 places charge on the diffusion 26 from the supply voltage Vdd. This charge is drained through the photodiode 21 at a rate proportional to the intensity of incident light on the photodiode 21. A signal proportional to this intensity can be read from the cell 11 on the dataline DL_m by enabling the access transistor 24.

During normal operation, the voltage Vdd supplied to the drain of the reset transistor 22 is common to every cell 11 (i.e. pixel) in the array 10. Each row 1 to n of cells 11 simultaneously receives a reset enable signal RRE_1 to RRE_n respectively via a row reset line 14_1 to 14_n. The reset enable signals RRE_1 to RRE_n are active when at a logical high and all have the same amplitude which may be substantially at the level of the supply voltage Vdd. Again, during normal operation, the voltage level 13 associated with this logical high is common throughout the array. This means that all diffusions 26 acting as capacitors are reset to the same level, ie the same amount of reset charge is placed on the node of the photodiode 21 for every cell 11.

The common reset voltage Vdd ensures that each cell 11 will respond in a similar manner if illuminated by light of a similar intensity. This is ideal for image capture operations but may cause large currents to be produced in the cell 11 substrates during reset particularly when the charges on the cells 11 have been substantially depleted in the radiation sensing cycle.

Referring to figure 3, there is shown a diagram of the image sensor array 30 in accordance with the present invention. In accordance with this embodiment, the reset enable signals RRE_1 to RRE_n which are generated in a row reset controller 31 are applied to lines 14_1 to 14_n to reset the sensor circuits 11. However, rather then generate simultaneous signals RRE_1 to RRE_n, they are sequentially generated in an appropriate order such that all cells are not reset simultaneously. In this way, only one or more rows are pre-reset at the same time which will generate tolerable currents in the substrate at any one time. Further in accordance with the present invention, once all of the rows have been pre-reset, the row reset controller 31 will generate simultaneous signals RRE_1 to RRE_n on the lines 14_1 to 14_n to reset all of the sensor circuits 11 to substantially the same voltage level. In the process, large currents will not be generated since all of the cells 11 will have a charge very nearly at the reset voltage prior to being globally reset. During the pre-reset process, the cells 11 are roughly charged to the same voltage level, however, variations occur mainly due to the integration time between the pre-resetting of individual rows at the different times. During the simultaneous reset process, the voltage supplied to the drain of the reset transistor 22 is common to every cell 11 on the array 30. The gate of each reset transistor 22 is driven by a common reset enable signal RRE_1 to RRE_n, each row 1 to n of cells 11 receives the same reset enable signal via a row reset line 14_1 to 14_n. This means that every cell 11 in the array 30 is reset to the same level or that the same amount of reset charge is placed on a node of the photodiode 21 for every cell 11. This common reset voltage ensures that each cell 11 will respond in a similar manner if illuminated by a light of similar intensity.

The above embodiment provides for the operation of an array 30 in which latch-up is avoided without increasing the cost of manufacturing or the use of space on the chip which would be necessitated with the addition of wells or biasing circuits for the array 30.

The sequence of pre-resetting the cells 11 in an array 30 may take many forms. For instance, individual cells 11 may be pre-reset individually or in groups, and a group of cells 11 need not be made up of adjacent cells 11. In addition, the cells 11 may be pre-reset in groups of one or more rows or one or more columns, and once again, the rows or columns need not be adjacent. Because of the integration of this APS array 30 with peripheral circuitry and other circuits, it is desirable to keep current flow at a fairly steady level, where large variations in current flow may disrupt other functioning circuits.

In a further embodiment of the present invention illustrated in figure 4, the array 40 is similar to the embodiment illustrated in figure 3 except that it includes a substrate voltage detector 41 which is connected to the row reset controller 31. The substrate voltage detector 41 tests the amount of charge (or voltage level) on the array 40 substrate. If charge levels are low, the row reset controller 31 will pre-reset more than one row at a time in order to reduce the integration time and power used to pre-reset and reset the entire array 40. The substrate voltage detector 41 may be in the form of a sensing circuit which compares the bias voltage level with a common signal such as ground. Such a circuit can determine the additional bias voltage that the array 40 is able to handle. This data can be used by the controller 41 to set the pre-reset/reset cycle of the array 40 so as to pre-reset a maximum number of cells 11 at a time. In addition, the controller 31 may be programmed to pre-reset selected numbers of adjacent or non-adjacent individual cells 11, as well as non-adjacent rows or columns.

The present invention can also be applied to variations of the active pixel sensor array, such as variations in the structure of the active pixel sensor. For example, a 4T or 5T structure can be employed, where a global reset is necessary in order to acquire a proper image.

While the invention has been described according to what is presently considered to be the most practical and preferred embodiments, it must be understood that the invention is not limited to the disclosed embodiments. Those ordinarily skilled in the art will understand that various modifications and equivalent structures and functions may be made without departing from the spirit and scope of the invention as defined in the claims. Therefore, the invention as defined in the claims must be accorded the broadest possible interpretation so as to encompass all such modifications and equivalent structures and functions.

What is claimed is:

1. A method of resetting an array of active pixel sensors (APS) arranged in rows and columns, comprising the steps of:

(a) pre-resetting the sensors in the array by sequentially resetting groups of one or more sensors; and

(b) resetting all of the sensors at one time.

2. A method as claimed in claim 1 wherein each group comprises one or more rows of sensors.

3. A method as claimed in claim 1 wherein each group comprises one or more columns of sensors.

4. A method as claimed in claim 1 wherein step (a) includes:

(a.i) detecting the bias voltage level of the sensor array;

(a.ii) selecting the number of sensors in the pre-resetting groups as a function of the bias voltage detected.

5. Apparatus for resetting an array of active pixel sensors (APS) arranged in rows and columns, comprising:

(a) a controller having means coupled to the sensor array for sequentially pre-resetting groups of one or more sensors in the array; and

(b) the controller having means coupled to the sensor array for simultaneously resetting all of the sensors in the array.

6. Apparatus as claimed in claim 5 which further includes:

(c) detector for detecting the bias voltage of the sensor array; and

(d) the controller being coupled to the voltage detector for determining sensors in each group being pre-reset.

7. Apparatus as claimed in claim 6 wherein each group comprises one or more rows of sensors.

8. Apparatus as claimed in claim 6 wherein each group comprises one or more columns of sensors.

Abstract

The method and apparatus for resetting an Active Pixel Sensor (APS) array comprises a controller for sequentially pre-resetting groups of one or more sensors in the array and then simultaneously resetting all of the sensors. The groups may be formed from one or more adjacent or non-adjacent individual sensors, rows or columns of sensors. The apparatus may further include a detector for sensing the bias voltage present on the array substrate in order for the controller to determine the number of sensors in the groups being reset. This method and apparatus assure that current flow is kept at a fairly steady level to avoid large variations in current flow that may disrupt other functioning circuits on the substrate including latch-up.

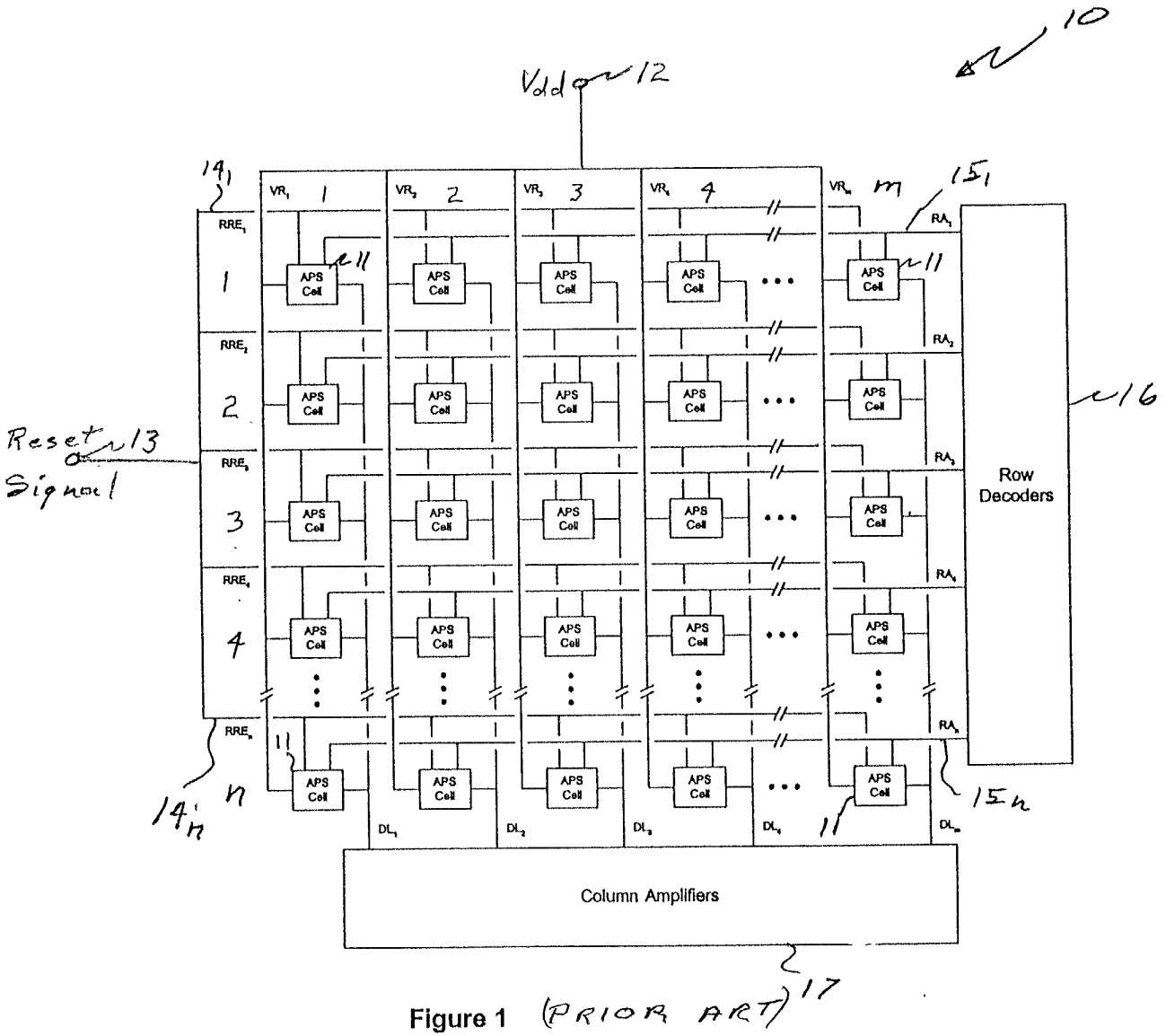

Figure 1 (PRIOR ART)

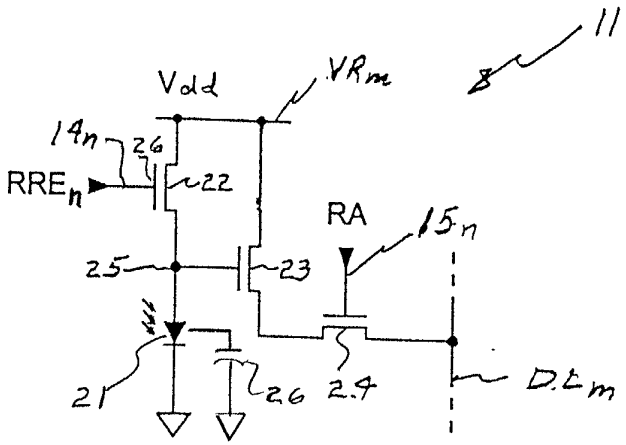

Figure 2 (PRIOR ART)

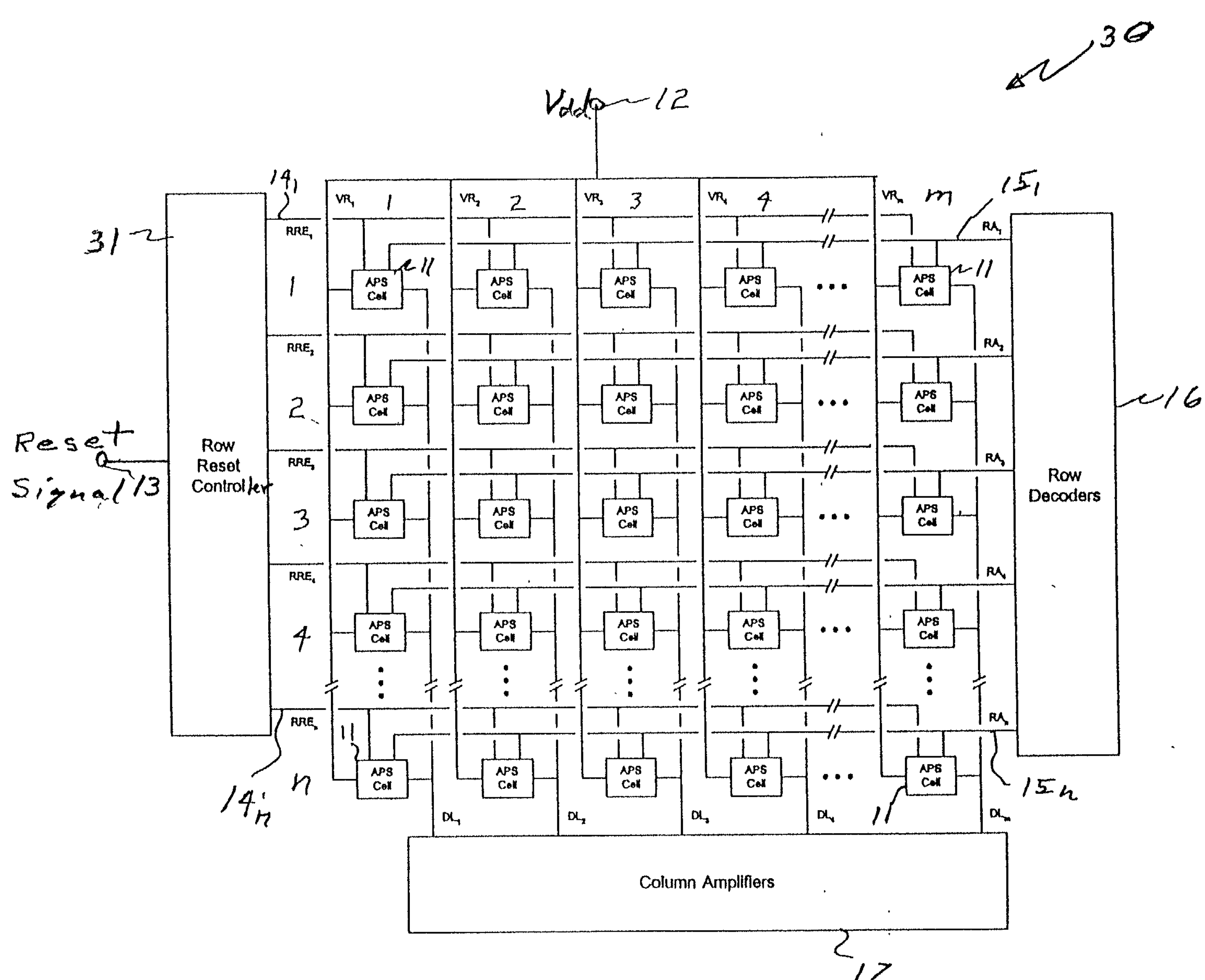
30
Vdd 12
31
Reset
Signal 13
Row
Reset
Controller
14₁
14'ₙ
RRE₁
RRE₂
RRE₃
RRE₄
RREₙ
1
2
3
4
n
VR₁
VR₂
VR₃
VR₄
VRₘ
m
APS
Cell
11
15₁
15ₙ
RA₁
RA₂
RA₃
RA₄
RAₙ
Row
Decoders
16
DL₁
DL₂
DL₃
DL₄
DLₘ
Column Amplifiers
17

Figure 3

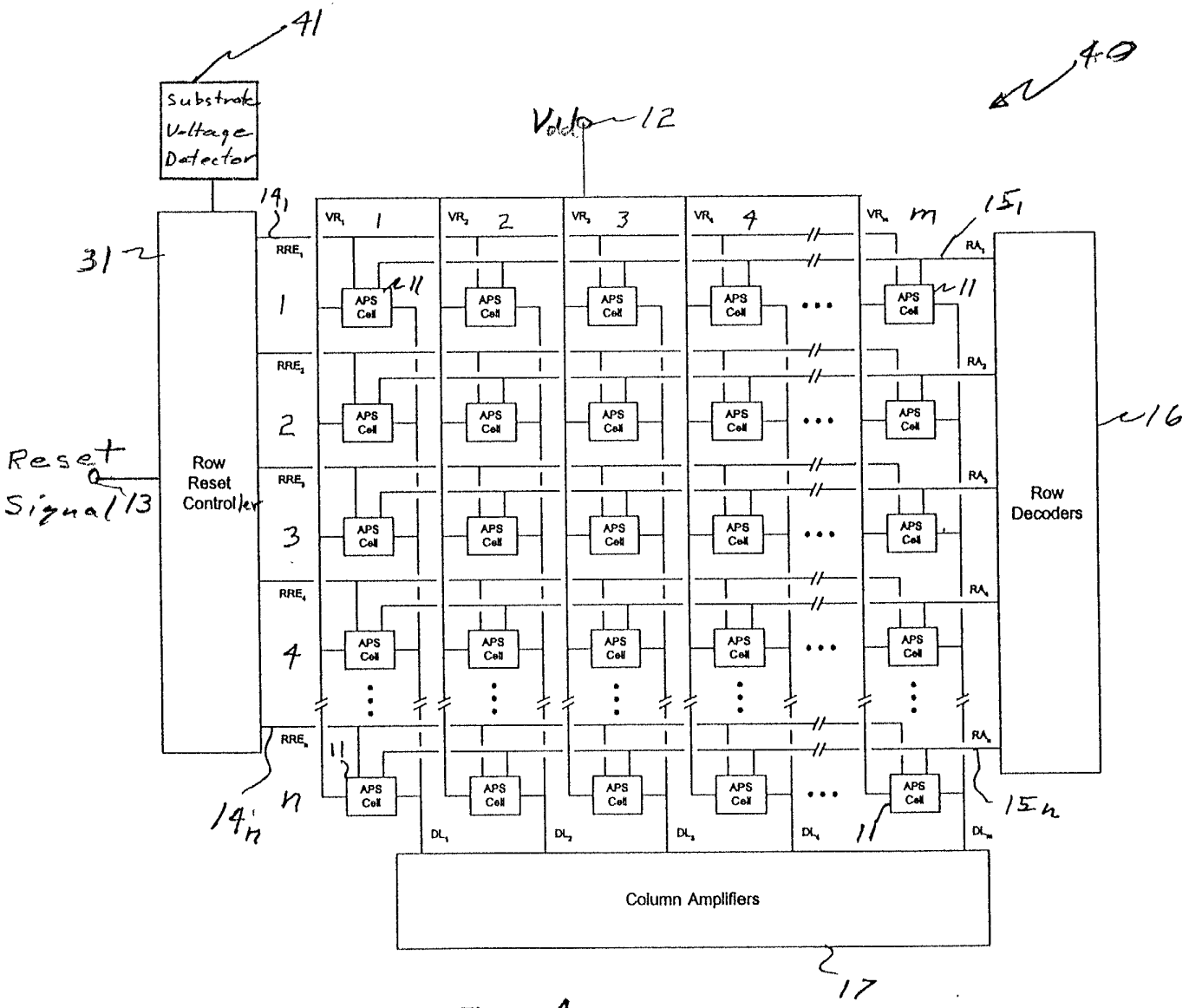

Figure 4

PATENT

COMBINED DECLARATION AND POWER OF ATTORNEY

ORIGINAL, DESIGN, NATIONAL STAGE OF PCT, SUPPLEMENTAL

As a below named inventor, I hereby declare that:

TYPE OF DECLARATION

This declaration is of the following type: Original

INVENTORSHIP IDENTIFICATION

My residence, post office address and citizenship are as stated below next to my name, I believe I am the original, first and sole inventor *(if only one name is listed below)* or an original, first and joint inventor *(if plural names are listed below)* of the subject matter which is claimed and for which a patent is sought on the invention entitled:

ACTIVE PIXEL SENSOR ARRAY RESET

SPECIFICATION IDENTIFICATION

the specification of which:

■ is attached hereto.

ACKNOWLEDGEMENT OF REVIEW OF PAPERS AND DUTY OF CANDOR

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations. § 1.56(a).

PRIORITY CLAIM

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed.

EARLIEST FOREIGN APPLICATION(S), IF ANY, FILED WITHIN 12 MONTHS
(6 MONTHS FOR DESIGN) PRIOR TO THIS U.S. APPLICATION

Country	**Application No.**	**Date of Filing** dd/mm/yyyy	**Priority Claimed Under 37 USC 119**

ALL FOREIGN APPLICATION(S), IF ANY, FILED MORE THAN 12 MONTHS
(6 MONTHS FOR DESIGN) PRIOR TO THIS U.S. APPLICATION

Country	**Application No.**	**Date of Filing**

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application Serial No.	**Filing Date**	**Status** (patented, pending, abandoned)

POWER OF ATTORNEY

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(List name(s) and registration number(s))*

Oliver W. Hayes, Registration No. 15,867
Norman P. Soloway, Registration No. 24,315
William O. Hennessey, Registration No.32,032
Susan H. Hage, Registration No. 29,646
Steven J. Grossman, Registration No. 35,001
~~Christopher K. Gagne, Registration No. 36,142~~

■ Attached as part of this declaration and power of attorney is the authorization of the above-named attorney(s) to accept and follow instructions from my representative(s).

SEND CORRESPONDENCE TO:

Hayes, Soloway, Hennessey & Hage
175 Canal Street
Manchester, New Hampshire
U.S.A. 03101

DIRECT TELEPHONE CALLS TO:
(Name and telephone number)

Norman P. Soloway
(603) 668-1400

DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such wilful false statements may jeopardize the validity of the application or any patent issued thereon.

SIGNATURE(s)

Full name of 1st inventor: **HUA, Paul**

Country of Citizenship: **People's Republic of China**

Residence Address: **308-58 Bayshore Drive, Nepean, Ontario, K2B 6M9, CANADA**

Post Office Address: **Same as Residence Address**

Date: July 12/00

Signature:

Full name of 2nd inventor: **HAUDEROWICZ, Peter**

Country of Citizenship: **Canada**

Residence Address: **210 Blackburn Avenue, Ottawa, Ontario, K1N 8A8, Canada**

Post Office Address: **Same as Residence Address**

Date: July 12/00

Signature: